Section I. (Amendments to the Claims)

Claims 25-49 are currently withdrawn from consideration.

Claims 10-16, 20, 22-23, 34-41, and 47 have been amended, as follows:

1. (Previously presented) A wafer susceptor for use in a substrate processing system, comprising:

   at least one recess formed therein, wherein each recess is arranged and configured to hold one substrate therein, wherein said at least one substrate comprises material selected from the group consisting of silicon, gallium nitride, and aluminum nitride, and wherein said water susceptor is characterized by physical properties that match those of the semiconductor substrates held therein.

2. (Previously presented) The wafer susceptor of Claim 1, wherein said at least one substrate comprises silicon.

3. (Previously presented) The wafer susceptor of Claim 1, wherein said physical properties comprise:

   Thermal coefficient of expansion;

   Reflectivity;

   Thermal mass;

   Thermal conductivity;

   Electrical resistivity;

   Dielectric constant;

   Dielectric loss;

   Density;

Hardness; and

Emissivity.

4. (Previously presented) A substrate processing system comprising at least one wafer susceptor as in claim 1, wherein said system further comprises an automated substrate transport assembly arranged for transporting substrates into and out of a deposition chamber in which said wafer susceptor is disposed.

5. (Previously presented) The substrate processing system of claim 4, wherein said automated substrate transport assembly is arranged for serially transporting single ones of a plurality of substrates into and out of said deposition chamber.

6. (Previously presented) The substrate processing system of claim 4, further comprising a substrate cassette for storage and bulk transport of plural arrays of substrates, and said substrate cassette is positioned in substrate pickup and substrate delivery relationship to the automated substrate transport assembly.

7. (Previously presented) The substrate processing system of claim 6, wherein said automated substrate transport assembly comprises a wand array comprising a plurality of wands constructed and arranged to simultaneously transport a corresponding plurality of substrates into and out of the deposition chamber, wherein the automated substrate transport assembly and the substrate cassette are constructed and arranged so that when the automated substrate transport assembly is translated into a pickup position relative to the substrate cassette, said plurality of wands engage and extract a plurality of substrates from the substrate cassette, with each wand engaging and extracting a substrate from a different one of said plural arrays of substrates, and so that when the automated substrate

transport assembly is translated into a deposit position relative to the substrate cassette, said plurality of wands release and deposit a plurality of substrates on the substrate cassette, with each wand releasing and depositing a substrate into a different one of said plural arrays of substrates.

8. (Previously presented) The substrate processing system of claim 4, wherein said automated substrate transport assembly comprises a double-sided wand array comprising a plurality of wands constructed and arranged to simultaneously transport a corresponding plurality of substrates into and out of the deposition chamber.

9. (Previously presented) The substrate processing system of claim 4, further comprising a loadlock chamber including a multiparted substrate cassette therein, and a transport arm arranged to selectively engage said multiparted substrate cassette and disengage from said multiparted substrate cassette in the loadlock chamber.

10. (Currently amended) A substrate processing system comprising at least two wafer ~~holders~~ susceptors as in claim 1, an etch chamber for regeneration of wafer ~~holders~~ susceptors, and an automated transport assembly arranged to (1) introduce one of said at least two wafer ~~holders~~ susceptors into a deposition chamber, while another of said at least two wafer ~~holders~~ susceptors is disposed in said etch chamber and regenerated thereby, and (2) thereafter extract said at least two wafer ~~holders~~ susceptors respectively from the deposition chamber and etch chamber, followed by introduction of one of said at least two wafer ~~holders~~ susceptors into the etch chamber from the deposition chamber, and introduction of another of said at least two wafer ~~holders~~ susceptors into the deposition chamber from the etch chamber.

11. (Currently amended) The substrate processing system of claim 10, wherein at least one of the wafer ~~holders~~ susceptors has two recesses therein.

12. (Currently amended) The substrate processing system of claim 10, wherein at least one of the wafer ~~holders~~ susceptors has four recesses therein.

13. (Currently amended) The substrate processing system of claim 10, wherein at least one of the wafer ~~holders~~ susceptors has a diameter in the range of from about 200mm to about 350mm.

14. (Currently amended) The substrate processing system of claim 10, wherein at least one of the wafer ~~holders~~ susceptors has a diameter in the range of from about 200mm to about 300mm.

15. (Currently amended) The substrate processing system of claim 10, wherein each of the wafer ~~holders~~ susceptors comprises recesses having a diameter in the range of from about 100mm to about 150mm.

16. (Currently amended) The substrate processing system of claim 10, wherein each of the wafer ~~holders~~ susceptors comprises recesses having a diameter in the range of from about 100mm to about 125mm.

17. (Previously presented) The substrate processing system of claim 10, further comprising a substrate cassette including slot members for positioning substrates in plural arrays, and wherein successive arrays are in side-by-side relationship to one another.

18. (Previously presented) The substrate processing system of claim 17, wherein the substrate cassette is constructed and arranged for holding two arrays of substrates, wherein all substrates are planar and each respective substrate in a first array is generally coplanar with a corresponding respective substrate in a second array.

19. (Previously presented) The substrate processing system of claim 18, wherein the first and second arrays are parallel to one another.

20. (Currently amended) The substrate processing system of claim 10, further comprising an automated substrate transport assembly and a substrate cassette, wherein the wafer ~~holders~~ susceptors, the automated substrate transport assembly, and the substrate cassette are constructed and arranged to simultaneously process two substrates.

21. (Previously presented) The substrate processing system of claim 10, comprising a single wafer deposition chamber sized for processing single substrates having a 200mm diameter.

22. (Currently amended) The substrate processing system of claim 21, wherein each wafer ~~holder~~ susceptor is arranged and configured for placement inside said single wafer deposition chamber, and each wafer holder comprises a plurality of recesses for holding substrates having a 100mm diameter.

23. (Currently amended) The substrate processing system of claim 22, wherein each of the recesses in each wafer ~~holder~~ susceptor is circular.

24. (Previously presented) The substrate processing system of claim 20, further comprising a

processor for programmable operating the automated substrate transport assembly according to a cycle time program.

25. (Withdrawn) A method for increasing the throughput of a single substrate deposition chamber, said method comprising:

positioning in said single substrate deposition chamber a wafer susceptor having at least one recess formed therein, with each recess being arranged and configured to hold one substrate therein, wherein said at least one substrate comprises material selected from the group consisting of silicon, gallium nitride, and aluminum nitride, and wherein said water susceptor is characterized by physical properties that match those of the at least one substrate held therein.

26. (Withdrawn) The method of Claim 25, wherein said at least one substrate comprises silicon.

27. (Withdrawn) The method of Claim 25, wherein said physical properties comprise:

thermal coefficient of expansion;

reflectivity;

thermal mass;

thermal conductivity;

electrical resistivity;

dielectric constant;

dielectric loss;

density;

hardness; and

emissivity.

28. (Withdrawn) The method of claim 25, further comprising providing an automated substrate transport assembly including a wand array comprising a plurality of wands constructed and arranged to simultaneously transport a corresponding plurality of substrates into and out of the single substrate deposition chamber.

29. (Withdrawn) The method of claim 25, further comprising providing an automated substrate transport assembly arranged for serially transporting single ones of a plurality of substrates into and out of said single substrate deposition chamber.

30. (Withdrawn) The method of claim 25, further comprising providing an automated substrate transport assembly for transporting substrates into and out of said single substrate deposition chamber.

31. (Withdrawn) The method of claim 30, further comprising providing a substrate cassette for storage and bulk transport of plural arrays of substrates, wherein the cassette is positionable in substrate pickup and substrate delivery relationship to the automated substrate transport assembly.

32. (Withdrawn) The method of claim 31, wherein said automated substrate transport assembly comprises a wand array comprising a plurality of wands constructed and arranged to simultaneously transport a corresponding plurality of substrates into and out of the single substrate deposition chamber,

wherein said automated substrate transport assembly is first translated into a pickup position relative to the substrate cassette, so that the plurality of wands of said automated substrate transport assembly engage and extract a plurality of substrates from the substrate cassette, with each wand engaging and extracting a substrate from a different

one of the plural arrays of substrates in said substrate cassette;

wherein said automated substrate transport assembly subsequently carries the engaged and extracted substrates to the single substrate deposition chamber and releases the substrates into respective recesses in the wafer holder;

after deposition of thin film material on the substrates in the single substrate deposition chamber, yielding coated substrates, the automated substrate transport assembly extracts the coated substrates from the respective recesses in the wafer susceptor,

carries the extracted coated substrates, and releases the coated substrates to said substrate cassette or a second substrate cassette.

33. (Withdrawn) The method of claim 25, comprising using a double-sided wand assembly comprising a plurality of wands and arranged to simultaneously transport a corresponding plurality of substrates into and out of the single substrate deposition chamber.

34. (Withdrawn) The method of claim 25, comprising sequentially using multiple wafer ~~holders~~ susceptors, by positioning one of the multiple wafer ~~holders~~ susceptors in the single substrate deposition chamber for processing of wafers thereon, and concurrently regenerating another of said multiple wafer ~~holders~~ susceptors after it has been in the single substrate deposition chamber during processing of wafers thereon.

35. (Withdrawn) The method of claim 34, wherein said regenerating comprises etch processing of said another of said wafer ~~holders~~ susceptors.

36. (Withdrawn) The method of claim 25, wherein the wafer ~~holder~~ susceptor has two

recesses therein.

37. (Withdrawn) The method of claim 25, wherein the wafer ~~holder~~ susceptor has four recesses therein.

38. (Withdrawn) The method of claim 25, wherein the wafer ~~holder~~ susceptor has a diameter in the range of from about 200 mm to about 350 mm.

39. (Withdrawn) The method of claim 25, wherein the wafer ~~holder~~ susceptor has a diameter in the range of from about 200 mm to about 300mm.

40. (Withdrawn) The method of claim 38, wherein each of the recesses in said wafer ~~holder~~ susceptor has a diameter in the range of from about 100mm to about 150mm.

41. (Withdrawn) The method of claim 38, wherein each of the recesses in said wafer ~~holder~~ susceptor has a diameter in the range of from about 100mm to about 125mm.

42. (Withdrawn) The method of claim 25, further comprising providing a substrate cassette including slot members for positioning substrates in plural arrays, and wherein successive arrays are in side-by-side relationship to one another.

43. (Withdrawn) The method of claim 25, further comprising providing a substrate cassette that is constructed and arranged for holding two arrays of substrates, wherein all substrates are planar and each respective substrate in a first array is generally coplanar with a corresponding respective substrate in a second array.

44. (Withdrawn) The method of claim 43, wherein the first and second arrays are parallel to one another.

45. (Withdrawn) The method of claim 25, further comprising providing an automated substrate transport assembly and a substrate cassette, wherein the single substrate deposition chamber, the automated substrate transport assembly, and the substrate cassette are constructed and arranged to simultaneously process two substrates.

46. (Withdrawn) The method of claim 25, wherein the single wafer deposition chamber is sized for processing single substrates having a 200mm diameter.

47. (Withdrawn) The method of claim 46, wherein the wafer ~~holder~~ susceptor comprises a plurality of recesses arranged and configured to hold substrates having a 100mm diameter.

48. (Withdrawn) The method of claim 47, wherein each of the recesses is circular.

49. (Withdrawn) The method of claim 25, further comprising providing an automated substrate transport assembly for transporting substrates into and out of the single substrate deposition chamber, and programmably operating the automated substrate transport assembly according to a cycle time program.

50. (Previously presented) A wafer susceptor used in a semiconductor substrate processing system, comprising at least one recess formed therein, wherein each recess is arranged and configured to hold one semiconductor substrate therein, wherein said at least one semiconductor substrate comprises material selected from the group consisting of silicon,

gallium nitride, aluminum nitride, diamond, gallium arsenide, indium nitride, indium phosphide, and gallium phosphide, wherein said wafer susceptor is characterized by physical properties that match those of the semiconductor substrates held therein.

51. (Previously presented) A wafer susceptor arranged and configured for placement in a single substrate deposition chamber, wherein said wafer susceptor is substantially circular in shape and comprises two or more recesses formed therein, wherein each recess is arranged and configured to hold one substrate, and wherein said water susceptor is characterized by physical properties that match those of the substrates held therein.

52. (Previously presented) The wafer susceptor of claim 51, wherein the substrates comprise material selected from the group consisting of silicon, GaN, SiC, and AlN.

REMARKS

§112 Rejections of Claims 10, 11, 13, and 20-23

The Examiner's rejections of claims 10, 11, and 20-23 under 35 U.S.C. §112, second paragraph, for lack of antecedent basis have been overcome by amendments of claims 10, 11, and 20-23 herein. Further, the informality of claim 13 has been overcome by corresponding amendment of such claim.

§102 and §103 Rejections of Claims 1-24 and 50-52

In the August 25, 2003 Final Office Action, the Examiner finalized the previously rejections of claims 1-24 and 50-52 under 35 U.S.C. §102(e) and/or 35 U.S.C. §103(a) as being unpatentable over **Suda** et al. U.S. Patent No. 6,053,980 (hereinafter "**Suda**"), or further in view of Nygaard U.S. Patent No. 3,765,763 (hereinafter "**Nygaard**").

Claim 1, from which claims 2-24 depend, recites:

> "A wafer susceptor for use in a substrate processing system, comprising:
>
> at least one recess formed therein, wherein each recess is arranged and configured to hold one substrate therein, wherein said at least one substrate comprises material selected from the group consisting of silicon, gallium nitride, and aluminum nitride, and **wherein said water susceptor is characterized by physical properties that match those of the substrates held therein**."

Claims 50 and 51 (from which claim 52 depends) correspondingly recite "A wafer susceptor… **wherein said wafer susceptor is characterized by physical properties that match those of the… substrates held therein**."

Suda, the primary reference cited by the Examiner, discloses a wafer susceptor comprising at least one recess arranged and configured for holding one substrate. Specifically, Suda discloses that the wafer susceptor can be made of a heat resistant material, such as quartz or glass (see Suda, column 23, lines 27-36, and column 16, lines 9-13), and that the substrate can be a glass substrate for a liquid crystal display element and the like (see Suda, column 31, lines 14-15).

<u>There is nothing in Suda *expressly* teaches or suggests use of a wafer holder that has physical properties that match with those of the substrate to be processed. Suda does not appreciate in any manner, or even acknowledge, the advantages of using such a property-matching wafer holder.</u>

Nevertheless, the Examiner asserted that the general disclosure by Suda, specifically the disclosure regarding use of <u>glass</u> for fabricating a <u>substrate holding means</u> and the disclosure regarding use of a <u>glass substrate</u>, amounts to *an inherent teaching* for constructing the substrate holding means by using a material "characterized by physical properties that match those of the substrate," as required by claim 1 of the present application (see the Final Office Action, Section 7(i)(b)), on the basis that (1) if the **<u>composition</u>** is physically the same, it must have the same properties, and (2) a **<u>chemical composition</u>** and its properties are inseparable (see the Final Office Action, Section 7(iii), citing In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990)).

Applicant respectfully disagrees with the Examiner's assertion and the associated reasoning, for the following reasons:

First, the term "**<u>glass</u>**" is defined as "any of **<u>a large class of materials with highly variable mechanical and optical properties</u>** that solidify from the molten state without crystallization, [are] typically made by silicates fusing with boric oxide, aluminum oxide, or phosphorus pentoxide, [are] generally hard, brittle, and transparent or translucent, and [are] considered to be supercooled liquids rather than true solids" (see The American Heritage® Dictionary of the English Language: Fourth Edition (2000) at <u>http://www.bartleby.com/61/35/G0143500.html</u>, as visited on October 10, 2003).

In other words, **<u>glass materials can have not only fundamentally different physical properties, but also fundamentally different chemical compositions</u>**. For example, certain low emissivity glass is characterized by an <u>emissivity</u> of lower than 0.2 (see <u>http://www.windowstoday.co.uk/warm_a_glass.htm</u>, as visited on October 10, 2003), while ordinary window glass has an <u>emissivity</u> of about 0.84 (see <u>http://www.glassguys.com/freeinfoArc.html</u>, as visited on October 10, 2003); normal glass composed of silica (<u>SiO_2</u>) has high <u>electrical resistivity</u> within the range of from about 1e+09 Ω*m (=1×10^{11} Ω*cm) to about

3.98e+11 Ω*m (=3.98×10^{13} Ω*cm) (see http://www.memsnet.org/material/glasssio2bulk/, as visited on October 10, 2003), but the resistivity of semiconducting glass consisting essentially of La_2O_3, B_2O_3, and Fe_2O_3 is reduced to within the range of from about 1×10^8 Ω*cm to about 1×10^{12} Ω*cm (see Fine U.S. Patent No. 5,158,812), and the resistivity of conductive glass made of Na_2O, Al_2O_3, ZrO_2, and SiO_2 is further reduced to less than 200 Ω*cm (see Nelson et al. U.S. Patent No. 4,659,637); further, the normal glass (i.e., plate glass) made of SiO_2, the borosilicate glass, and the BVC (i.e., black vitrified ceramic) glass are characterized by significantly different thermal coefficient of expansion, thermal conductivity, hardness, and reflectivity (see http://pages.infinit.net/asmprod/techinfo.html, as visited on October 10, 2003).

Therefore, **the general disclosure by Suda regarding use of glass for forming the substrate holding means and the use of glass substrate does not teach or suggest in any manner that the substrate holding means and the substrate are formed of the same, or even similar, type of glass material**, and **Suda thus does not provide any derivative basis for a wafer susceptor having the same or identical chemical composition as that of the substrate**, despite the assertions by the Examiner on page 4, lines 6-9 of the Final Office Action, **much less a wafer susceptor "characterized by physical properties that match those of the substrates held therein," as required by all the pending claims of the present application**.

Second, **inherency may not be established by probability or possibilities**. *In re Oelrich*, 212 USPQ 323, 326 (CCPA 1981). The mere fact that a certain thing may result from a give set of circumstances is insufficient to establish inherency and anticipation. *In re Weiss*, 26 USPQ2d 1885, 1888 (Fed. Cir. 1993). To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference must be filled with extrinsic evidence that makes it clear that the missing descriptive matter is **necessarily present** in the thing described in the reference and that it would be so recognized by persons of ordinary skill. *Continental Can Co. USA v. Monsanto Co.*, 20 USPQ2d 1746 (Fed. Cir. 1991).

Therefore, the remote possibility that a person ordinarily skilled in the art, after reading Suda, could conceivably, in the realm of all possibilities, use the same glass material of same chemical composition and therefore match physical properties for forming the heat resistant substrate holder and for forming the glass substrate for liquid crystal display element, is not sufficient to establish inherency and anticipation of Applicant's claimed invention by Suda. Instead, for proof

of inherency and anticipation, such use of the same glass material for both the substrate and the substrate holder would have to be necessarily present in the disclosure by the Suda reference.

However, nothing in Suda discloses or suggests, either expressly or implicitly, that the substrate and the substrate holder are formed of the same glass material, or glass materials of similar chemical compositions, or glass materials of similar physical properties, and it is clear that a substrate holder characterized by physical properties that match those of the substrate, as required by Applicant's claimed invention in pending claims 1-52, is **not necessarily present** in the disclosure by the Suda reference.

Thus, **the disclosure of Suda does not anticipate Applicant's claimed invention, either directly or inherently**.

Finally, in light of the lack of any appreciation by Suda regarding the advantages of using property-matching wafer susceptor for holding wafer substrate, **a person ordinarily skilled in the art, after reading Suda, would not have been motivated to make a wafer susceptor of physical properties that match those of the substrate, as required by all the pending claims of the present application**. It is therefore clear that Applicant's claimed invention is not obvious over the Suda reference.

Nothing in the newly cited Nygaard reference remedy such deficiency by Suda.

Applicant's claimed invention, as recited in pending claims 1-52, thus patentably distinguishes both cited references, Suda and Nygaard, either taken singularly or in combination, and the Examiner is hereby requested to reconsider, and upon consideration to withdraw, the rejections of such claims.

Conclusion

Claims 1-52 as amended/added herein are fully patentably distinguished over the cited reference, and in form and condition for allowance. Issue of a Notice of Allowance for the application is therefore requested.

The Office is hereby authorized to charge any fees that are necessary for entry of this Response and credit any excess payment to Deposit Account No. 08-3284 of Intellectual Property/Technology Law.

If any issues remain outstanding, incident to the formal allowance of the application, the Examiner is requested to contact the undersigned attorney at (919) 419-9350 to discuss same, in order that this application may be allowed and passed to issue at an early date.

Respectfully submitted,

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APPENDIX A

Clean Copy of All Pending Claims

1. A wafer susceptor for use in a substrate processing system, comprising:

   at least one recess formed therein, wherein each recess is arranged and configured to hold one substrate therein, wherein said at least one substrate comprises material selected from the group consisting of silicon, gallium nitride, and aluminum nitride, and wherein said water susceptor is characterized by physical properties that match those of the semiconductor substrates held therein.

2. The wafer susceptor of Claim 1, wherein said at least one substrate comprises silicon.

3. The wafer susceptor of Claim 1, wherein said physical properties comprise:

   Thermal coefficient of expansion;

   Reflectivity;

   Thermal mass;

   Thermal conductivity;

   Electrical resistivity;

   Dielectric constant;

   Dielectric loss;

   Density;

   Hardness; and

   Emissivity.

4. A substrate processing system comprising at least one wafer susceptor as in claim 1, wherein said system further comprises an automated substrate transport assembly

arranged for transporting substrates into and out of a deposition chamber in which said wafer susceptor is disposed.

5. The substrate processing system of claim 4, wherein said automated substrate transport assembly is arranged for serially transporting single ones of a plurality of substrates into and out of said deposition chamber.

6. The substrate processing system of claim 4, further comprising a substrate cassette for storage and bulk transport of plural arrays of substrates, and said substrate cassette is positioned in substrate pickup and substrate delivery relationship to the automated substrate transport assembly.

7. The substrate processing system of claim 6, wherein said automated substrate transport assembly comprises a wand array comprising a plurality of wands constructed and arranged to simultaneously transport a corresponding plurality of substrates into and out of the deposition chamber, wherein the automated substrate transport assembly and the substrate cassette are constructed and arranged so that when the automated substrate transport assembly is translated into a pickup position relative to the substrate cassette, said plurality of wands engage and extract a plurality of substrates from the substrate cassette, with each wand engaging and extracting a substrate from a different one of said plural arrays of substrates, and so that when the automated substrate transport assembly is translated into a deposit position relative to the substrate cassette, said plurality of wands release and deposit a plurality of substrates on the substrate cassette, with each wand releasing and depositing a substrate into a different one of said plural arrays of substrates.

8. The substrate processing system of claim 4, wherein said automated substrate transport

assembly comprises a double-sided wand array comprising a plurality of wands constructed and arranged to simultaneously transport a corresponding plurality of substrates into and out of the deposition chamber.

9. The substrate processing system of claim 4, further comprising a loadlock chamber including a multiparted substrate cassette therein, and a transport arm arranged to selectively engage said multiparted substrate cassette and disengage from said multiparted substrate cassette in the loadlock chamber.

10. A substrate processing system comprising at least two wafer susceptors as in claim 1, an etch chamber for regeneration of wafer susceptors, and an automated transport assembly arranged to (1) introduce one of said at least two wafer susceptors into a deposition chamber, while another of said at least two wafer susceptors is disposed in said etch chamber and regenerated thereby, and (2) thereafter extract said at least two wafer susceptors respectively from the deposition chamber and etch chamber, followed by introduction of one of said at least two wafer susceptors into the etch chamber from the deposition chamber, and introduction of another of said at least two wafer susceptors into the deposition chamber from the etch chamber.

11. The substrate processing system of claim 10, wherein at least one of the wafer susceptors has two recesses therein.

12. The substrate processing system of claim 10, wherein at least one of the wafer susceptors has four recesses therein.

13. The substrate processing system of claim 10, wherein at least one of the wafer susceptors

has a diameter in the range of from about 200mm to about 350mm.

14. The substrate processing system of claim 10, wherein at least one of the wafer susceptors has a diameter in the range of from about 200mm to about 300mm.

15. The substrate processing system of claim 10, wherein each of the wafer susceptors comprises recesses having a diameter in the range of from about 100mm to about 150mm.

16. The substrate processing system of claim 10, wherein each of the wafer susceptors comprises recesses having a diameter in the range of from about 100mm to about 125mm.

17. The substrate processing system of claim 10, further comprising a substrate cassette including slot members for positioning substrates in plural arrays, and wherein successive arrays are in side-by-side relationship to one another.

18. The substrate processing system of claim 17, wherein the substrate cassette is constructed and arranged for holding two arrays of substrates, wherein all substrates are planar and each respective substrate in a first array is generally coplanar with a corresponding respective substrate in a second array.

19. The substrate processing system of claim 18, wherein the first and second arrays are parallel to one another.

20. The substrate processing system of claim 10, further comprising an automated substrate

transport assembly and a substrate cassette, wherein the wafer susceptors, the automated substrate transport assembly, and the substrate cassette are constructed and arranged to simultaneously process two substrates.

21. The substrate processing system of claim 10, comprising a single wafer deposition chamber sized for processing single substrates having a 200mm diameter.

22. The substrate processing system of claim 21, wherein each wafer susceptor is arranged and configured for placement inside said single wafer deposition chamber, and each wafer holder comprises a plurality of recesses for holding substrates having a 100mm diameter.

23. The substrate processing system of claim 22, wherein each of the recesses in each wafer susceptor is circular.

24. The substrate processing system of claim 20, further comprising a processor for programmable operating the automated substrate transport assembly according to a cycle time program.

25. A method for increasing the throughput of a single substrate deposition chamber, said method comprising:

positioning in said single substrate deposition chamber a wafer susceptor having at least one recess formed therein, with each recess being arranged and configured to hold one substrate therein, wherein said at least one substrate comprises material selected from the group consisting of silicon, gallium nitride, and aluminum nitride, and wherein said water susceptor is characterized by physical properties that match those of the at least one

substrate held therein.

26. The method of Claim 25, wherein said at least one substrate comprises silicon.

27. The method of Claim 25, wherein said physical properties comprise:

thermal coefficient of expansion;

reflectivity;

thermal mass;

thermal conductivity;

electrical resistivity;

dielectric constant;

dielectric loss;

density;

hardness; and

emissivity.

28. The method of claim 25, further comprising providing an automated substrate transport assembly including a wand array comprising a plurality of wands constructed and arranged to simultaneously transport a corresponding plurality of substrates into and out of the single substrate deposition chamber.

29. The method of claim 25, further comprising providing an automated substrate transport assembly arranged for serially transporting single ones of a plurality of substrates into and out of said single substrate deposition chamber.

30. The method of claim 25, further comprising providing an automated substrate transport

assembly for transporting substrates into and out of said single substrate deposition chamber.

31. The method of claim 30, further comprising providing a substrate cassette for storage and bulk transport of plural arrays of substrates, wherein the cassette is positionable in substrate pickup and substrate delivery relationship to the automated substrate transport assembly.

32. The method of claim 31, wherein said automated substrate transport assembly comprises a wand array comprising a plurality of wands constructed and arranged to simultaneously transport a corresponding plurality of substrates into and out of the single substrate deposition chamber,

wherein said automated substrate transport assembly is first translated into a pickup position relative to the substrate cassette, so that the plurality of wands of said automated substrate transport assembly engage and extract a plurality of substrates from the substrate cassette, with each wand engaging and extracting a substrate from a different one of the plural arrays of substrates in said substrate cassette;

wherein said automated substrate transport assembly subsequently carries the engaged and extracted substrates to the single substrate deposition chamber and releases the substrates into respective recesses in the wafer holder;

after deposition of thin film material on the substrates in the single substrate deposition chamber, yielding coated substrates, the automated substrate transport assembly extracts the coated substrates from the respective recesses in the wafer susceptor,

carries the extracted coated substrates, and releases the coated substrates to said substrate

cassette or a second substrate cassette.

33. The method of claim 25, comprising using a double-sided wand assembly comprising a plurality of wands and arranged to simultaneously transport a corresponding plurality of substrates into and out of the single substrate deposition chamber.

34. The method of claim 25, comprising sequentially using multiple wafer susceptors, by positioning one of the multiple wafer susceptors in the single substrate deposition chamber for processing of wafers thereon, and concurrently regenerating another of said multiple wafer susceptors after it has been in the single substrate deposition chamber during processing of wafers thereon.

35. The method of claim 34, wherein said regenerating comprises etch processing of said another of said wafer susceptors.

36. The method of claim 25, wherein the wafer susceptor has two recesses therein.

37. The method of claim 25, wherein the wafer susceptor has four recesses therein.

38. The method of claim 25, wherein the wafer susceptor has a diameter in the range of from about 200 mm to about 350 mm.

39. The method of claim 25, wherein the wafer susceptor has a diameter in the range of from about 200 mm to about 300mm.

40. The method of claim 38, wherein each of the recesses in said wafer susceptor has a

diameter in the range of from about 100mm to about 150mm.

41. The method of claim 38, wherein each of the recesses in said wafer susceptor has a diameter in the range of from about 100mm to about 125mm.

42. The method of claim 25, further comprising providing a substrate cassette including slot members for positioning substrates in plural arrays, and wherein successive arrays are in side-by-side relationship to one another.

43. The method of claim 25, further comprising providing a substrate cassette that is constructed and arranged for holding two arrays of substrates, wherein all substrates are planar and each respective substrate in a first array is generally coplanar with a corresponding respective substrate in a second array.

44. The method of claim 43, wherein the first and second arrays are parallel to one another.

45. The method of claim 25, further comprising providing an automated substrate transport assembly and a substrate cassette, wherein the single substrate deposition chamber, the automated substrate transport assembly, and the substrate cassette are constructed and arranged to simultaneously process two substrates.

46. The method of claim 25, wherein the single wafer deposition chamber is sized for processing single substrates having a 200mm diameter.

47. The method of claim 46, wherein the wafer susceptor comprises a plurality of recesses arranged and configured to hold substrates having a 100mm diameter.

48. The method of claim 47, wherein each of the recesses is circular.

49. The method of claim 25, further comprising providing an automated substrate transport assembly for transporting substrates into and out of the single substrate deposition chamber, and programmably operating the automated substrate transport assembly according to a cycle time program.

50. A wafer susceptor used in a semiconductor substrate processing system, comprising at least one recess formed therein, wherein each recess is arranged and configured to hold one semiconductor substrate therein, wherein said at least one semiconductor substrate comprises material selected from the group consisting of silicon, gallium nitride, aluminum nitride, diamond, gallium arsenide, indium nitride, indium phosphide, and gallium phosphide, wherein said wafer susceptor is characterized by physical properties that match those of the semiconductor substrates held therein.

51. A wafer susceptor arranged and configured for placement in a single substrate deposition chamber, wherein said wafer susceptor is substantially circular in shape and comprises two or more recesses formed therein, wherein each recess is arranged and configured to hold one substrate, and wherein said water susceptor is characterized by physical properties that match those of the substrates held therein.

52. The wafer susceptor of claim 51, wherein the substrates comprise material selected from the group consisting of silicon, GaN, SiC, and AlN.

The American Heritage® Dictionary of the English Language: Fourth Edition. 2000.

glass

PRONUNCIATION: glăs

NOUN: **1.** Any of a large class of materials with highly variable mechanical and optical properties that solidify from the molten state without crystallization, are typically made by silicates fusing with boric oxide, aluminum oxide, or phosphorus pentoxide, are generally hard, brittle, and transparent or translucent, and are considered to be supercooled liquids rather than true solids. **2.** Something usually made of glass, especially: **a.** A drinking vessel. **b.** A mirror. **c.** A barometer. **d.** A window or windowpane. **3a. glasses** A pair of lenses mounted in a light frame, used to correct faulty vision or protect the eyes. **b.** A binocular or field glass. Often used in the plural. **c.** A device, such as a monocle or spyglass, containing a lens or lenses and used as an aid to vision. **4.** The quantity contained by a drinking vessel; a glassful. **5.** Objects made of glass; glassware.

ADJECTIVE: **1.** Made or consisting of glass. **2.** Fitted with panes of glass; glazed.

VERB: Inflected forms: **glassed, glass·ing, glass·es**

TRANSITIVE VERB: **1a.** To enclose or encase with glass. **b.** To put into a glass container. **c.** To provide with glass or glass parts. **2.** To make glassy; glaze. **3a.** To see reflected, as in a mirror. **b.** To reflect. **4.** To scan (a tract of land or forest, for example) with an optical instrument.

INTRANSITIVE VERB: **1.** To become glassy. **2.** To use an optical instrument, as in looking for game.

ETYMOLOGY: Middle English *glas*, from Old English *glæs*. See **ghel-**[2] in Appendix I.